Supplementary Material for:

Beyond equivalent circuit representations in nonlinear systems with inherent memory

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As presented in the manuscript, and based on Refs. [A,B], the most basic mechanism for the generation of a memristive response is the perturbed Drude conductance

$$I = (G_0 + \gamma\, \delta n)\, V,$$

with $\gamma = e\mu/d^2$ determined by the elementary change e, the carrier mobility, μ, and the distance between contacts, d. The dynamics of non-equilibrium carriers can be emulated under the relaxation time approximation as

$$\frac{d\delta n}{dt} = -\frac{\delta n}{\tau} + g(V).$$

By adopting the viewpoint elucidated in the manuscript, we can construct a circuit model that mimics the behavior of a memristor across diverse conditions, particularly focusing on the regime of small amplitude approximation. In this context, the generation-trapping function can be effectively approximated up to second order on the applied voltage

$$g(V) = \sigma_o V + \sigma_e V^2,$$

where σ_o and σ_e encapsulate the microscopic details pertaining to carrier generation or trapping, thereby exhibiting the potential for assuming distinct signs. This approach reduces the essential *apparent* components, as represented in Figure 1S, necessary to accurately replicate memristive loops. It is important to note that adopting a multimode perspective is imperative for accurately replicating the memory response, as described in the manuscript. Therefore, the incorporation of multipliers and rectifiers in the *apparent* circuit becomes unavoidable in order to achieve this goal. The circuit components are determined by the values of σ_o, σ_e, γ , τ, and the voltage amplitude, according to the expressions detailed in the manuscript. As emphasized in the paper, they can take on positive or negative values depending on the nature of the function g(V), making it impossible to attribute any concrete physical significance to them beyond the *apparent* perspective. Figure 2S showcases a collection of memristive loops generated through various parameter sets defining the apparent circuit elements.

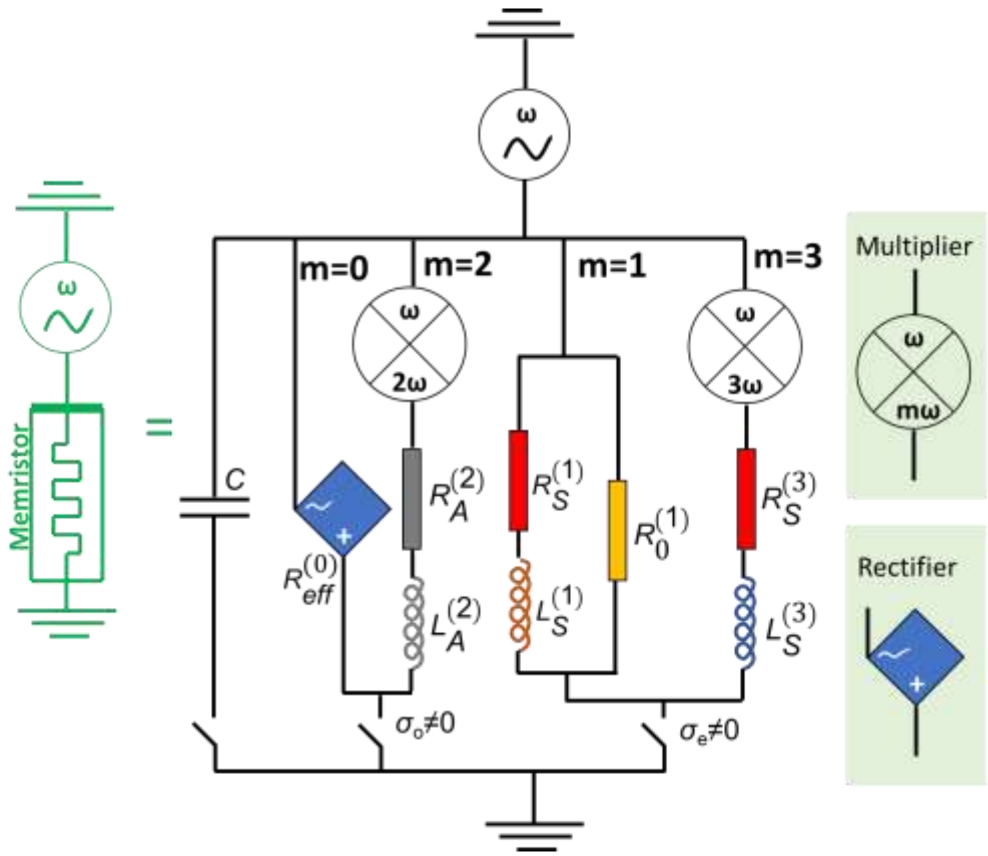

Figure 1S: *Equivalent* circuit containing the minimal basic ingredients to reproduce a memristive response under small amplitude condition.

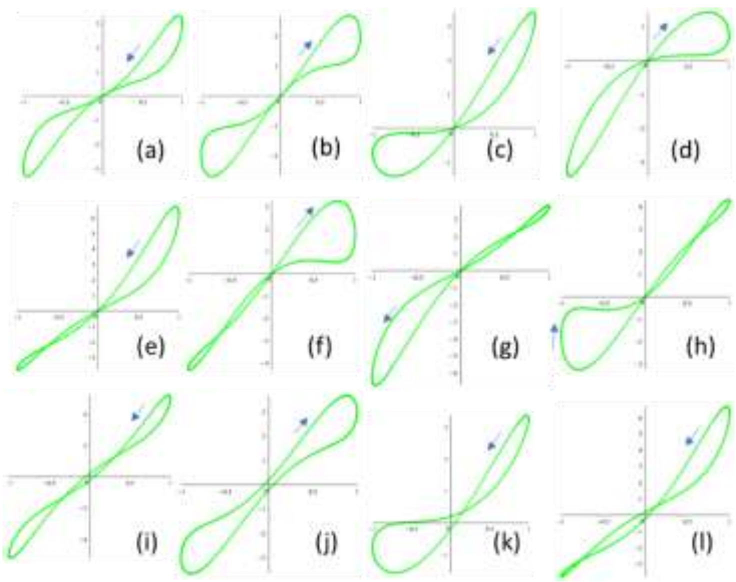

Figure 2S: Potential memristive loops mimicked under different combinations of parameters of the apparent circuit in Figure 1S: (a) C=0, $\sigma_o=0$, and $\sigma_e>0$ (b) C=0, $\sigma_o=0$, and $\sigma_e<0$ (c) C=0, $\sigma_o>0$, and $\sigma_e=0$ (d) C=0, $\sigma_o<0$, and $\sigma_e=0$ (e) C=0, $\sigma_o>0$, and $\sigma_e>0$ (f) C=0, $\sigma_o<0$, and $\sigma_e<0$ (g) C=0, $\sigma_o<0$, and $\sigma_e>0$ (h) C=0, $\sigma_o>0$, and $\sigma_e<0$ (i) C≠0, $\sigma_o=0$, and $\sigma_e>0$ (j) C≠0, $\sigma_o=0$, and $\sigma_e<0$ (k) C≠0, $\sigma_o>0$, and $\sigma_e=0$ (l) C≠0, $\sigma_o>0$, and $\sigma_e>0$

In scenarios involving simultaneous and independent switching mechanisms, expanding the apparent circuits becomes straightforward by just incorporating parallel segments. Each segment includes the circuit elements corresponding to the respective generation function, denoted as, $g_j(V)$, as represented in Figure 3S.

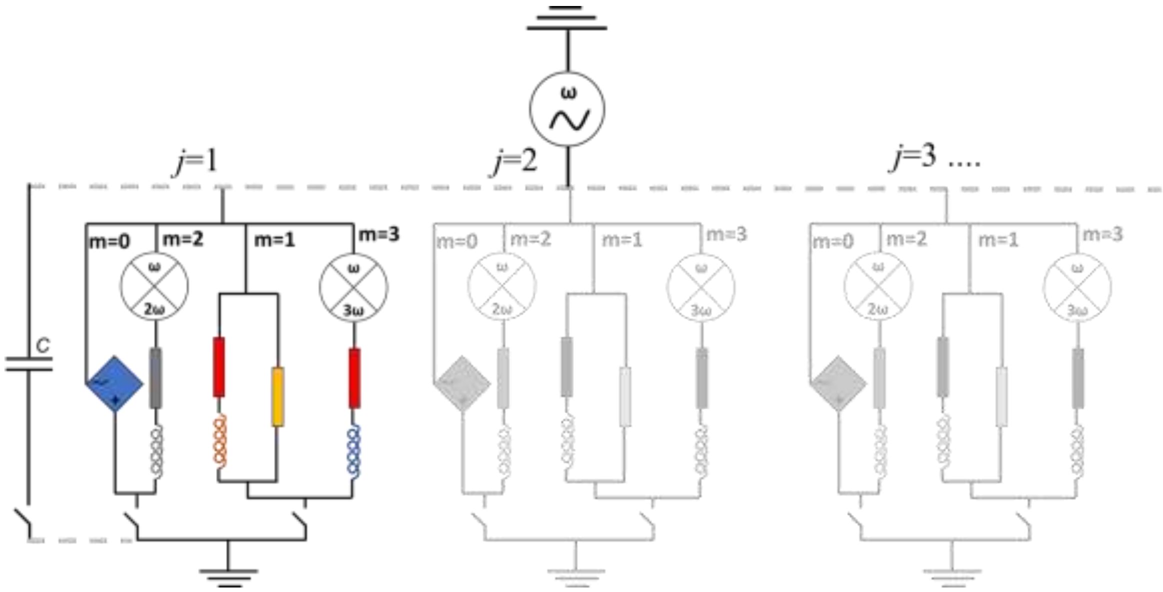

Figure 3S: Extension of the equivalent circuit of a memristive response by assuming the coexistence of *j*=1,2,3… independent switching mechanisms.

References

[A] R. S. W. Silva, F. Hartmann, and V. Lopez-Richard, *The Ubiquitous Memristive Response in Solids*. IEEE Transactions on Electron Devices 69, 5351 (2022).

[B] V. Lopez-Richard, R. S. W. Silva, O. Lipan, and F. Hartmann, *Tuning the conductance topology in solids*. Journal of Applied Physics 133, 134901 (2023).